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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,682	06/09/2000	Sheila M. Rader	CS-10246	3605

7590 01/11/2005

Motorola inc
Personal Communications Sector
Intellectual Property Department (MCS)
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Libertyville, IL 60048

EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/591,682	RADER ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-16,29,31-34 and 38-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-16,29,31-34 and 38-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 5-16, 29, 31-34, 38-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 9-10, 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Iimura et al EP 446855 A2.

In regards to claims 1, 9-10, 29: Iimura teaches A data transfer system comprising: a plurality of peripheral interfaces (61-68); a first memory (11); a programmable direct memory access module (A and B taken together) coupling the first memory to each of the plurality of peripheral interfaces (61-68), wherein the programmable direct memory access module configures selectively programmable direct memory access data channels (channel 1-8) between the first memory (11) and, respectively, each one of the plurality of peripheral interfaces (61-68); a first processor (10) coupled to the programmable direct memory access module (A,B) and associated with the first memory (11) through a first shared bus (12), which couples both the first processor (10) and the first memory (11) to the programmable direct memory access module (A,B); a second memory (3) coupled to the programmable direct memory access module (A,B),

wherein the programmable direct memory access module (A,B) configures the selectively programmable direct memory access data channels (Channels 1-8) between the second memory (3) and respectively, each one of the plurality of peripheral interfaces (61-68); and a second processor (4) coupled to the programmable direct memory access module (A,B) and associated with the second memory (3) through a second shared bus (5), independent of the first share bus (12), which couples both the second processor (4) and the second memory (3) to the programmable memory access module (A,B).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8, 11-16, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iimura et al EP 446855 A2 in view of Yokoyama et al PN 5,678,060.

In regards to claims 5, 12: Iimura teaches establishing a channel between the memory 3 and the interfaces. Iimura is silent on what the interfaces are attached to. Yokoyama et al teaches establishing channels between a computer 1 through an interface to any of identical computers 1A to 1D. It would have been obvious to attach the interfaces of Iimura to identical external computers because this would have allowed for multiprocessing in Iimura as well as given the interfaces of Iimura a purpose. The examiner notes with identical computers being attached to the interfaces of Iimura any of the external computers processors and memory would

map to applicants claimed first processor and memory. Thus Host 4 of the attached identical computer is the first processor and memory 3 of the attached identical computer is the first memory.

In regards to claim 6: Iimura teaches the DMA including a programmable processor (10).

In regards to claim 7: Iimura teaches the DMA including a line controller (8).

In regards to claims 8, 11, 14, 31: Iimura teaches the DMA including a scheduler (channel selector 7 working in conjunction with line control circuit 8). Iimura however does not expressly teach the scheduler using a priority scheme. Yokoyama teaches prioritizing data e.g. col. 15, lines 11-40; col. 17, lines 14-40. It would have been obvious to a person of ordinary skill in the art at the time of the invention to prioritize the data because this would have different types of communications.

In regards to claim 13: Yokoyama teaches receiving a timed request for a DMA transfer (col. 10 lines 18-67).

In regards to claim 15 and 16, Yokoyama discloses the method of interrupting and resuming the transferring of data in the event a higher priority DMA data transfer is required (col. 7, lines 30-35).

In regards to claim 31: Iimura teaches the use of channel control registers (81-88 and 91-98).

6. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iimura et al EP 446855 in view of what is well known in the art as evidenced by Zampini et al H1752.

In regards to claim 32: Iimura teaches the DMA controller as described above. Iimura does not state that the DMA controller is a digital signal processor DMAC. Zampini et al teaches the well known feature of a DSP DMA. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a have the DMA controller of Iimura be a DSP DMAC because this would have allowed to external devices such as sensors and graphics processors.

In regards to claim 33: Iimura teaches multiple DMA channels (Figure 1a) as well as handling multiple virtual DMA channels (Figure 4).

In regards to claim 34: Iimura teaches embedded RAM's.

7. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iimura et al EP 446855 in view of Grant et al PN 4,805,137.

In regards to claims 38-41: Iimura teaches multiple channel configuration registers (81-88 and 91-98). Iimura also teaches the registers control such items as number of bytes and address (which could be considered as the claimed pointer register). Iimura does not expressly teach other well known values such as enable and override. Grant teaches a DMA including pointer registers, enable and override. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include these well known DMA controls because this would have allowed for priority control and well as disabling channels when they are not used.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

PRM
January 6, 2005